the fourth step of forming a first conductive film electrically connected to one of said impurity diffusion layers;

the fifth step of forming a mask pattern having at least first and second openings on said first conductive film;

E' contd

the sixth step of etching said first conductive film by using said mask pattern as a mask until said first opening divides said first conductive film in said first opening below said second opening above said isolation structure, and simultaneously forms a recess in said second opening having said first conductive film forming a bottom of said recess;

the seventh step of forming a dielectric film so as to cover a surface of said first conductive film; and

the eighth step of forming a second conductive film on said dielectric film opposing said first conductive film through said dielectric film.

36. (Amended) A method of fabricating a semiconductor device, comprising:

the first step of forming a first conductive film in an insulating film region on a semiconductor substrate;

the second step of forming a mask pattern having two openings of different dimensions on said first conductive film;

the third step of etching said first conductive film by using said mask pattern as a mask, thereby dividing said first conductive film conforming to a shape of one of said

E2

openings so as to reach said insulating film region, forming a cylindrical hole below said second opening in which a surface of said insulating film region is exposed, and simultaneously forming at least one recess in a surface of said divided first conductive film conforming to a shape of the other opening;

the fourth step of forming an insulating film so as to cover a surface of said first conductive film; and

the fifth step of forming a second conductive film so as to cover a surface of said insulating film opposing said first conductive film through said insulating film.

38. (Amended) A method of fabricating a semiconductor device, comprising:

the first step of defining an element active region by forming an element isolation structure on a semiconductor substrate;

the second step of forming an insulating film on said semiconductor substrate in said element active region;

the third step of forming a first conductive film on an entire surface including said insulating film and said element isolation structure;

the fourth step of forming a mask pattern having at least first and second openings on said first conductive film;

E3

the fifth step of etching said first conductive film until said element isolation structure is exposed in said first and second openings by using said mask pattern as a mask, thereby dividing said first conductive film below said first opening, and simultaneously forming a cylindrical hole extending through said first conductive film below said second opening and said first conductive film is etched until said insulating layer is exposed in said first opening;

the sixth step of forming a dielectric film so as to cover said first conductive film; and

the seventh step of forming a second conductive film on said dielectric film and opposing said first conductive film through said dielectric film.

REMARKS

Claims 28-36, 38-42, 44 and 45 are pending in the application.

Claims 28-31, 42, 44 and 45 are allowed.

Claims 32-36 and 38-41 are rejected. Favorable reconsideration of the rejected claims is requested in light of the foregoing amendments hereto.

Withdrawal of the rejection of claims 32-34 and 36, under 35 U.S.C. §102(e) as being anticipated by Schoenfeld et al. (U.S. Pat. No. 6,010,932), is requested.